REMARKS

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Amendments and Support for Same

In response to the Examiner contention that the term "a layout design" in claim 1 is interpreted as a noun, Applicant has amended the claim to add recite "prior to performing a layout design". No new matter has been added.

According to MPEP 608.01(o), "a term used in the claims may be given a special meaning in the description". Further, according to MPEP §2111.02 (III), Applicant may be own lexicographer. According to the specification, a process of a performing a layout design is shown in a flow diagram "SUB2" as shown in, e.g., Fig. 4, and is described in the present application.

Applicant respectfully invites the Examiner to review the application again, wherein it is shown at least, e.g., Figs. 3 and 5, and their respective disclosure in the specification, for support for the features of claim 1. In Fig. 1, reference numeral 26 denotes a circuit design functional unit, and reference numeral 30 denoting a clock generating functional part.

Further, Applicant's invention as recited in claim 2 includes the layout design functional unit (block 28 of Fig. 1) that follows sequentially the above-mentioned circuit design functional unit (block 26 of Fig. 1 and a high-level diagram in Fig. 2) of claim 1. Fig. 4 shows the layout design routine performed in block 28 of Fig. 1. The steps of claim 2 are directed to the layout design routine in Fig. 2 and Fig. 4.

Accordingly, claims 1-5 are respectfully submitted for consideration. Approval and entry of the amendments are respectfully requested.

2. Objection to the Claims

With respect to the objection to claim 1, Applicant respectfully submits that there is no contradiction between the second step and the recitation of "at least the first and second steps are performed prior to a layout design of the semiconductor integrated circuit" in amended claim 1. As explained in the specification, Applicant's claimed second step is

found in, e.g., Fig. 3, as step SS20 of SUB1 in a circuit design routine, while Applicant's claimed feature of performing a layout design is a separate routine having a combination of steps shown in, e.g., Fig. 4 as SUB2. Hence, the claimed steps are clear and enabling without any contradiction alleged by the Examiner.

In view of the amendment and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of the objection to claim 1.

3. Rejection under 35 U.S.C. §102(e)

With respect to the rejection of claims 1-5 under 35 U.S.C. §102(e) as being anticipated by Sano (US 2004/0107408), Applicant respectfully traverses the rejection at least for the reason that Sano fails describe each and every limitation recited in the rejected claims.

Amended claim 1 recites, among other features, the optimization of the timings being repeated according to the violation of the constraints of timings and at least the first and second steps being performed prior to performing a layout design of the semiconductor integrated circuit. That is, the steps in SUB1 in Fig. 3 are performed before the steps in SUB2 in Fig. 4.

In the rejection of claim 1, the Examiner alleges that Fig. 21 of Sano shows "at least the first and second steps are performed prior to a layout design of the semiconductor integrated circuit" without pointing which of the numerous features shown in Fig. 21 of Sano anticipates Applicant's claimed features. However, Applicant cannot find support for the allegation, and respectfully submits that Sano describes a different invention than that of Applicant's claimed invention. Should the Examiner maintain this allegation, Applicant would respectfully request the Examiner to provide concrete support and to clarify the rejection by pointing out which feature of Fig. 21 of Sano is relevant or pertinent to Applicant's aforementioned claimed feature.

Further, Applicant respectfully submits that claim 1 of the present invention recites a number of steps taken in a sequence and combination that constitutes a process. The steps in, e.g., Fig. 21 of Sano alleged as equivalent to Applicant's claimed steps do not follow the sequential order and combination as Applicants' claimed steps. That is, the Examiner selected various features of Sano that are not relevant to Applicant's claimed steps and

mischaracterized as equivalent to Applicant's claimed steps.

For example, Sano teaches inserting a buffer having a size which makes groups of element satisfy a fan-out restriction. However, Applicant's invention is different from Sano, and there is no steps claimed in Applicant's invention that relates to a method of inserting buffers having a size which makes groups of element satisfy a fan-out restriction as described by Sano.

Page 4, second paragraph of the present specification and the Abstract of the Disclosure discuss known technique of inserting buffer blocks in signal paths to change signal delay value that appears similar to Sano's method. The specification of the present invention also discusses the problems with inserting buffer blocks in signal paths to effect signal delays.

Further, Applicant respectfully submits that the design of integrate circuit is often involves minimizing clock skew. However, Sano does not teach the sequence or combination at least first, second, and third steps of Applicant's claim 1 and the fourth, fifth, sixth, and seventh steps of claim 2, for example.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in Sano, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-5, under 35 U.S.C. §102(e), as anticipated by Sano is improper.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to consider Sano in its entirety as set forth in MPEP 2141.02(VI) when applying Sano in the §102(e) rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §102(e) rejection of claims 1-5.

4. Conclusion

In view of the amendments to the claims, and in further view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-5 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Respectfully submitted,

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